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10/758,857	01/16/2004	Karsten Meyer-Grafe	2133.015USU	6567

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EXAMINER	
CONTINO, PAUL F	
ART UNIT	PAPER NUMBER
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/758,857	MEYER-GRAFE ET AL.	
	Examiner	Art Unit	
	PAUL F. CONTINO	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION: Non-Final Rejection

Response to Arguments

1. Applicant's arguments filed August 13, 2008, have been fully considered but are not persuasive.

The Examiner respectfully disagrees with the Applicant's arguments regarding the prior art reference Yoshida as failing to teach of the invention as claimed. In order to more clearly illustrate how the Yoshida reference parallels the Applicant's invention, the Examiner invites the Applicant to consider the parallels apparent between the invention as described in the Specification on page 3 lines 17-26, page 3 line 34 through page 4 line 3, page 6 line 26 through page 7 line 1, and page 7 lines 14-15, including Figure 1 elements #11 and S_1, with the Yoshida reference disclosure column 1 lines 13-62 and Figure 5. Both the Applicant's disclosure and the Yoshida reference describe and illustrate two process signals identifying a same event being inputted redundantly into an AND logic in order to convert the two signals into a single process signal to be further operated on to determine whether or not a fault exists. As claimed and in light of the Applicant's disclosure, the applied prior art by the Examiner sufficiently and adequately coincides with the Applicant's invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 9, 11-15, 19, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshida (U.S. Patent No. 6,356,821).

As in claim 1, Yoshida discloses a method for transmission of safe process information, comprising:

detecting a first process signal for identifying an event that is relevant to system safety *Fig. 5 #51; column 1 lines 13-33, where the signal output from microcomputer 51 is in response to a braking event from a signal event 50)*;

detecting at least one more process signal redundantly for identifying the same event *(Fig. 5 #51,52,57; column 1 lines 53-55, where the result signals from 51 and 52 are redundantly detected by comparing circuit 57, in response to the same braking event from a signal event 50)*;

converting said first and at least one more process signals to a single process signal for further system-based processing to carry out logic operations on a single-signal basis for

identifying the same event *(Fig. 5 #57,OUT; column 1 lines 53-62, where the output of comparing circuit 57 is a single fault signal which is inherently processed logically in order to determine if it is necessary to halt the processing system)*,

wherein the single process signal comprises process information that indicates a fault free behavior with regard to the same event only when said first and at least one more process signals indicate a fault free behavior with regard to said event *(Fig. 5 #57,OUT; column 1 lines 53-62, where the output of comparing circuit 57 contains process information indicating a fault if there is a fault and fault free behavior if not)*.

As in claim 2, Yoshida discloses said redundantly detected process signals are detected in said conversion process via two or more channels, and wherein said single process signal is transmitted via one channel *(Fig. 5; two channels, one each from microcomputers 51 and 52, respectively, and a signal process signal output on a signal channel from comparing circuit 57)*.

As in claim 3, Yoshida discloses said detection process is in digital or analog form *(Fig. 5; column 1, where it is inherent that the detection is in digital or analog form)*.

As in claim 4, Yoshida discloses said conversion process is carried out to form a digital process signal *(Fig. 5 #57; where logic AND gate 57 inherently forms a digital signal output)*.

As in claim 5, Yoshida discloses transmitting a 1-bit data item as the useful content of said single process signal *(Fig. 5 #57; column 1 lines 53-62, where the output of logic AND gate converter 57 is inherently a 1-bit item, which is used for determining a fault)*.

As in claim 9, Yoshida discloses said conversion process is carried out at a point in a process signal transmission path capable of being predetermined *(Fig. 5 #57; column 1, where the conversion is predetermined to occur at circuit 57)*.

As in claim 11, Yoshida discloses an apparatus for safe transmission of process signals, comprising:

a plurality of process signals being supplied on two or more channels and detected redundantly to identify the same event relevant to system safety *(Fig. 5 #51,52,57; column 1 lines 53-55, where the result signals from 51 and 52 are redundantly detected by comparing circuit 57, in response to the same braking event from a signal event 50)*; and

a converter for conversion of said plurality of process signals to a single process signal, said single process signal being capable of being transmitted via one channel to carry out [[the]] logic representations on a single-signal basis to identify said event *(Fig. 5 #57,OUT; column 1 lines 53-62, where the output of comparing circuit 57 is a single fault signal which is inherently processed logically in order to determine if it is necessary to halt the processing system)*, wherein said converter converts the single process signal so as to include process information that indicates a fault free behavior with regard to the same event only when said plurality of process signals indicate a fault free behavior with regard to said event *(Fig. 5 #57,OUT; column*

1 lines 53-62, where the output of comparing circuit 57 contains process information indicating a fault if there is a fault and fault free behavior if not).

As in claim 12, Yoshida discloses means for system-based further processing of said single process signal *(Fig. 5 #57; column 1 lines 55-62, where the output of comparing circuit 57 is inherently further processed in order to halt operation of the processing system).*

As in claim 13, Yoshida discloses said converter has associated with it an input component, an output component, an intelligent unit, and a mechatronic unit *(Fig. 5).*

As in claim 14, Yoshida discloses said converter is capable of producing a 1-bit data item *(Fig. 5 #57; a logic AND gate inherently produces a 1-bit data output).*

As in claim 15, Yoshida discloses said converter comprises a logic AND gate *(Fig. 5 #57; element 57 is illustrated as a logic AND gate).*

As in claim 19, Yoshida discloses said converter comprises hardware and/or software elements *(Fig. 5; column 1, where it is inherent that the converter 57 comprises hardware and/or software elements).*

As in claim 20, Yoshida discloses at least one network for an automation system *(Fig. 5; column 1; where the vehicle, ABS, and ECU are an automation system network).*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 6-8 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Emde et al. (U.S. PGPub 2003/0115543).

As in claim 6, Yoshida teaches of a single process signal. However, Yoshida fails to teach that transmission of said single process signal is protected. Emde et al. teaches transmission of a protected process signal *(paragraphs [0007]-[0008], where the CRC check bits are a form of signal protection)*.

It would have been obvious for a person skilled in the art at the time the invention was made to have included the signal protection as taught by Emde et al. in the invention of Yoshida. This would have been obvious because protection of signals upon transmission ensures corrupt data is detected for safety-assurance (paragraph [0004]). Further, both the inventions of Yoshida and Emde et al. relate to safety-related processes occurring in a vehicle *(Yoshida: column 1 lines 14-15; Emde et al.: paragraph [0004])*.

As in claim 7, Yoshida teaches of a single process signal with useful content. However, Yoshida fails to teach of check bits. Emde et al. teaches of attaching check bits to useful content *(paragraphs [0007]-[0008], where the CRC check bits are attached to the useful content message)*.

It would have been obvious for a person skilled in the art at the time the invention was made to have included the check bits as taught by Emde et al. in the invention of Yoshida. This would have been obvious because use of check bits with signals upon transmission ensures corrupt data is detected for safety-assurance (paragraph [0004]). Further, both the inventions of Yoshida and Emde et al. relate to safety-related processes occurring in a vehicle *(Yoshida: column 1 lines 14-15; Emde et al.: paragraph [0004])*.

As in claim 8, Emde et al. teaches of using a CRC method to produce said at least one check bit *(paragraph [0008])*.

As in claim 16, Yoshida teaches of a converter and a single process signal. However, Yoshida fails to teach of signal protection. Emde et al. teaches of a protected process signal *(paragraphs [0007]-[0008], where the CRC check bits are a form of signal protection; such protection may be included as part of a unit which includes a converter, such as the one taught by Yoshida)*.

It would have been obvious for a person skilled in the art at the time the invention was made to have included the signal protection as taught by Emde et la. in the invention of Yoshida. This would have been obvious because protection of signals upon transmission ensures corrupt

data is detected for safety-assurance (paragraph [0004]). Further, both the inventions of Yoshida and Emde et al. relate to safety-related processes occurring in a vehicle *(Yoshida: column 1 lines 14-15; Emde et al.: paragraph [0004])*.

As in claim 17, Emde et al. teaches means for generation of at least one check bit and for attachment of said at least one check bit to a signal content of said single process signal *(paragraphs [0007]-[0008], where the CRC check bits are generated and attached to the useful content message)*.

As in claim 18, Yoshida teaches of a converter. However, Yoshida fails to teach of a CRC method. Emde et al. teaches of application of a CRC method *(paragraph [0008])*.

It would have been obvious for a person skilled in the art at the time the invention was made to have included the CRC method as taught by Emde et al. in the invention of Yoshida. This would have been obvious because use of CRC with signals upon transmission ensures corrupt data is detected for safety-assurance (paragraph [0004]). Further, both the inventions of Yoshida and Emde et al. relate to safety-related processes occurring in a vehicle *(Yoshida: column 1 lines 14-15; Emde et al.: paragraph [0004])*.

* * *

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Kikuchi (U.S. Patent No. 4,794,601).

As in claim 10, Yoshida teaches of a signal process signal. However, Yoshida fails to teach of a single signal being converted to two or more additional process signals. Kikuchi teaches of a single signal being converted to two or more additional process signals that are carried via separate channels in a system output component that is capable of being predetermined *(Figs. 2 and 5; column 4 lines 6-42, specifically lines 32-34)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the signal conversion as taught by Kikuchi in the invention of Yoshida. This would have been obvious because the inclusion of multiple outputs as taught by Kikuchi allows for a fault tolerant operating environment *(column 4 lines 43-49)*.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL F. CONTINO whose telephone number is (571)272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Scott T Baderman/
Supervisory Patent Examiner, Art Unit 2114

PFC
11/3/2008